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Research/Work Interests

Computer architecture, multi-core architectures, simulation systems.

Education

01/2003 – 09/2007: *University of California, San Diego*.
Ph.D. in Computer Science.

09/2000 – 01/2003: *University of California, Irvine*.
Attended Ph.D. program in the Information and Computer Science program, transfered to UCSD later on.

03/1998 – 07/2000: *Federal University of Minas Gerais(UFMG), Brazil*.
M.S. in Computer Science.

03/1994 – 12/1997: *Pontifical Catholic University of Minas Gerais, Brazil*.
B.S. in Computer Science.

Work Experience

12/2007 – present: *Intel Corporation, Santa Clara, CA*.
Position: Component Engineer

03/2006 – 08/2007: *Intel Corporation, Hudson, MA*.
Worked as an Intern with development of efficient capturing and simulation of multi-threaded shared memory applications.

06/2005 – 09/2005: *Intel Corporation, Hudson, MA*.
Worked as an Intern with development of deterministic execution of multi-threaded programs using binary instrumentation, to enable efficient simulation/checkpoint generation of multi-threaded workloads.

03/1999 – 08/2000: *Research Development Foundation (FUNDEP – http://www.fundep.ufmg.br)*.
Worked as a Software Engineer with development of embedded systems using pSOS RTOS and targeting a Motorola communication processor platform used in telecommunication equipment. The project was a research cooperation between the Federal University of Minas Gerais and Bosch Telecom Corporation. I was responsible for all the operating system related issues on the project.

06/1996 – 03/1998: *Audiolab Eletronic Systems, Brazil (www.audiolab.com.br)*.
Worked part-time as an intern in development of a distributed SCADA (Supervisory Control and Data Acquisition) real time system, using QNX operating system on a Desktop platform, in a research cooperation between the Federal University of Minas Gerais and Laboratory of Computer Engineering of the Computer Science Department of Federal University of Minas Gerais (http://www.lecom.dcc.ufmg.br).

Research Projects

Research on efficient hardware and software mechanisms to log share-memory dependencies for multi-core systems [1, 2].

Developed efficient logging and deterministic simulation techniques for reproducible application-level architecture simulation [3, 4].

Developed Cycle-Close simulation scheme, to enable the use of sampling techniques for dynamic power/performance estimation ofmicroprocessors [5].

Collaborated in the design of leakage aware algorithms for minimizing structural leakage energy consumption in embedded systems [6].

Collaborated in the development of a cross-layer energy optimization framework [7].

Developed a DVS and DPM APIs for power management of embedded systems and validated the code with the implementation of scheduling algorithms on embedded system hardware platforms [8, 9].

Developed a code generation and optimization framework for telecommunication systems specified in SDL (Specification and Description Language) [10, 11].

Teaching Experience

University of California, San Diego - Teaching Assistant
CSE 237a (Grad Level) Introduction to Embedded System (Fall 2005)

University of California, Irvine - Teaching Assistant
ICS 155 System Design Laboratory (Winter 2001, Spring 2002)
ICS 51 Introductory Computer Organization (Fall 2000)

Talks Given

Reproducible Simulation of Multi-Threaded Workloads for Architecture Design Exploration. *International Symposium on Workload Characterization (IISWC'08)*, September 2008, Seattle, USA.

Software Profiling for Deterministic Replay Debugging of User Code. *5th International Conference on Software Methodologies, Tools and Techniques*, October 2006, Quebec City, Canada.

Automatic Logging of Operating System Effects to Guide Application-Level Architecture Simulation. *SIGMETRICS - International Conference on Measurement and Modeling of Computer Systems*, June, 2006, Saint-Malo, France.

Dynamic Phase Analysis for Cycle-Close Trace Generation. *International Conference on Hardware/Software Codesign and System Synthesis*, September 2005, New Jersey, USA.

Integrating Preemption Threshold Scheduling and Dynamic Voltage Scaling for Energy Efficient Real-Time Systems. *10th International Conference on Real-Time and Embedded Computing Systems and Applications (RTCSA '04)*, June 2004, Gothenburg, Sweden.

Selected Papers

[1] Satish Narayanasamy, Cristiano Pereira, and Brad Calder. Recording shared memory dependencies for application-level replay debugging. In *12th International Conference on Architectural Support for Programming Languages and Operating Systems*, October 2006.

[2] Satish Narayanasamy, Cristiano Pereira, and Brad Calder. Software profiling for deterministic replay debugging of user code. In *5th International Conference on Software Methodologies, Tools and Techniques*, October 2006.

[3] Satish Narayanasamy, Cristiano Pereira, Harish Patil, Robert Cohn, and Brad Calder. Automatic logging of operating system to guide application-level architecture simulation. In *Sigmetrics - International Conference on Measurement and Modeling of Computer Systems*, June 2006.

[4] Cristiano Pereira, Harish Patil, and Brad Calder. Reproducible simulation of multi-threaded workloads for architecture design exploration. In *International Symposium on Workload Characterization (IISWC'08)*, September 2008.

[5] Cristiano Pereira, Jeremy Lau, Brad Calder, and Rajesh Gupta. Dynamic phase analysis for cycle-close trace generation. In *Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis*, pages 321–326, September 2005.

[6] Ravindra Jejurikar, Cristiano Pereira, and Rajesh Gupta. Leakage aware dynamic voltage scaling for real-time embedded systems. In *Proceedings of the 41st annual conference on Design automation (DAC)*, pages 275–280. ACM Press, 2004.

[7] Shivajit Mohapatra, Nalini Venkatasubramanian, Nikil Dutt, Cristiano Pereira, and Rajesh Gupta. *Ultra Low Power Electronics and Design*, chapter fourteen - Energy-Aware Adaptations for end-to-end video streaming to mobile handheld devices. Kluwer Academic Publishers, 2004.

[8] C. Pereira, R. Gupta, and M. Srivastava. Pasa: A software architecture for building power aware embedded systems. In *In the proceedings of the IEEE CAS Workshop on Wireless Communications and Networking - Power efficient wireless ad hoc networks*, California, USA, September 2002.

[9] V. Raghunathan, C. Pereira, M. B. Srivastava, and R. Gupta. Energy aware wireless systems with adaptive power-fidelity tradeoffs. *IEEE Transactions on VLSI Systems*, Accepted for publication in 2004.

[10] Cristiano Pereira et. al. JADE: An embedded systems specification, code generation and optimization tool. In *Proceedings of the XIII Symposium on Integrated Circuits and System Design*, pages 18–24, September 2000.

[11] Cristiano Pereira. Code generation and optimization for embedded systems specified in SDL (original text in portuguese). Master's thesis, Federal University of Minas Gerais (UFMG), Brazil, 2000.