

Research Interests

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1 Nanotechnology: Opportunities and Challenges

Nanotechnology, as originally mentioned early in Richard Feynman's talk "There's Plenty of Room at the Bottom" in 1959, has been widely acknowledged as one of today's most important evolving areas, possessing a high potential to become the momentum for the next generation of revolution in science and technology. As a new area that covers a wide variety of fields, nanotechnology is projected to initiate revolutionary changes and overcome previously insurmountable challenges in multiple disciplines, including material science, mechanical engineering, biology, bioengineering, medical science, electronic engineering, computer science & engineering, and so on [1, 2].

Particularly, in the field of electronic systems, Moore's law has driven the exponential shrinking of semiconductor transistor size for the past forty years. Currently, the dominating CMOS technology has reached 90 nanometers in scale, and according to the *International Technology Roadmap for Semiconductors (ITRS)*, the shrinking is projected to reach beyond 45 nanometers in scale by 2010 [3, 4]. When entering the nanometer scale, where quantum effects dominate, CMOS starts to meet its physical limits and further shrinking in the sizes of CMOS based transistors is therefore checkmated by the insurmountable barriers of quantum effect, leakage current and power consumption. A number of new nanoelectronic devices, based on the quantum physical effects, have been proposed as highly promising to continue the scaling down of transistor sizes into the nanometer scale. The substitution of CMOS transistors by nanoelectronic devices is expected to not only break the barrier to the further extension of Moore's law, but also open up huge vistas for future opportunities.

However, for nanoelectronics based systems, there is neither any existing solution to guarantee the success of constructing a workable one, nor any perceivable straightforward way to achieve the goal of exploiting the advantages presented in the underlying nanotechnology. The drastic changes at the fundamental level of devices might eventually necessitate an entirely new set of computational models to be established for the future nanoelectronic systems. Meanwhile, research at the device level has demonstrated that a number of nanoelectronic device candidates can be used to create operational transistors, which further support the construction of basic memory elements and logic gates. Such fast paced development at the device level has demanded impending research investigation on the construction of nanoelectronics based systems. To overcome the grand challenge of forming novel nanoelectronic systems according to the underlying new devices, yet within a foreseeable narrow time frame, it is instructive to refer to the valuable experiences developed throughout the four decades, in which the construction of electronic systems has gone through a series of device level evolutions. One of the basic principles that has remained constant, regardless of changes in device levels, is to resort to hierarchical design at well-defined points of abstraction to break down the complexity in constructing an electronic system. Since the effect of the shrinking size in nanoelectronic devices has certainly been boosting the number of transistors on a chip, such a hierarchical based design principle is expected to be even more important in dealing with the tremendous complexity involved in the future nanoelectronic system constructions.

For the current CMOS based electronic systems, well developed design methodologies and CAD approaches exist at multiple hierarchical levels: from the highest behavioral level synthesis down to the physical level placement and routing, and such design technologies certainly provide helpful reference points for the future nanoelectronic systems [5]. However, due to the significant differences at the device level and their further implications on all the design hierarchy levels, a number of fundamental questions need to be answered for the nanoelectronic systems to begin taking place in the near future:

- What are the new advantages and challenges exhibited by the emerging nanoelectronic devices?

- How do the device level differences between the new nanoelectronics and the current CMOS devices influence the system perspectives?
- What are the appropriate computational models at various design hierarchy levels for a nanoelectronics based system?
- Which part of the current design methodologies are applicable to the future nanoelectronics based systems?
- With the drastically different new nanoelectronic devices, how should workable systems be constructed despite the huge challenges imposed by the device characteristics, and furthermore exploiting the advantages provided by the nanoelectronics to deliver system optimizations?

2 Nanoelectronic Background

Although no single nanoelectronic device can be expected to replace CMOS for the next generation of transistors, a number of device candidates are promising, including Carbon Nanotube Electronics (CNT) [6], Resonant Tunnel Devices (RTD) [7], Quantum Cellular Automata (QCA) [8], Single-Electron Transistors (SET) [9, 10], Molecular devices [11, 12, 13, 14] and Spin devices [15]. Although each of the multiple candidates possesses its own specific characteristics, they do share a number of important characteristics, determined by their nanometer scale [3, 4].

- **Fabrication:** Current CMOS systems utilize top-down fabrication, which is limited in obtaining precision when scaling down to the nano level. Aggressive approaches in lithographic fabrication do exist for the nanoelectronic environment, yet they are too expensive to be applied for massive production. On the other hand, a bottom-up approach is expected to prevail as the basic way to construct nanoscale circuits by building structures in a self-assembly manner. The main implications of a bottom-up fabrication process are: 1) *regularity in structures* imposed by the self-assembly process, 2) *massive defects* caused during the fabrication process, and 3) *post-fabrication reconfigurability* necessitated to define the circuits and bypass the defects.
- **Interconnect:** Accessing the extremely small devices and delivering information at high speed and bandwidth is an essential challenge in the nanoelectronic environment. The small gain of the quantum devices strongly limits the number of fan-outs, while some devices, such as QCA, even rely on the interaction between neighboring devices to implement the transfer of signals. Interconnection essentially becomes the dominant issue in a nanoelectronic system in terms of area, delay and power consumption. Communications between geographically distant devices through nano wires is extremely expensive and *localized interconnection* becomes a critical criterion in the nanoelectronic environment.
- **Reliability:** The high unreliability of nanoelectronic devices exists mainly in two forms.
 - First, manufacturing defects increase significantly. The fabrication process in nano environments is prone to defects due to the small scale of devices and the bottom-up self-assembly process. In comparison with the defect rates of 10^{-9} to 10^{-7} in current CMOS systems, the defect rates of nanoelectronic systems are projected to be extremely high, of the order of 10^{-3} to 10^{-1} .
 - Second, a high occurrence of transient faults is expected during run-time. Due to the nanometer scale of devices which utilize ultra low voltage, nanoelectronic transistors tend to be highly sensitive to environmental influences, such as temperature, cosmic ray particles and background noise.

An increased number of transient faults have been observed in current CMOS based systems, as the device scales down to the deep sub-micron stage. In nanoelectronics based systems, the challenge of dynamic transient faults is furthermore severely aggravated. The ultra low power utilized, as well as the quantum effects nanoelectronic devices rely on, both result in significantly reduced noise margins and highly increased sensitivity to environmental effects. A large number of transient faults,

therefore, is expected to be triggered in the future nanoelectronic systems due to the environmental effects, such as variances in temperature, cosmic particles, background noises, and crosstalk effects.

Furthermore, in the nanoelectronic environment, not only is the fault rate projected to be high, but also a high variance in the fault rate and a clustered behavior of faults can be expected. The functionality of most nanoelectronic devices is extremely sensitive to a certain set of manufacturing parameters. However, the bottom-up manufacturing process cannot perfectly control such parameters to be precisely identical across all the devices fabricated, thus inevitably resulting in variations among the transistors. Such variations lead to significant differences in performance, robustness, as well as noise immunity among the devices in a chip, engendering clustered fault behavior in the system. Furthermore, such clustering behavior of the faults is exasperated by the factor that most environmental effects, including elevation in temperature generated by heavy computations, exhibit clustered behavior as well.

The identification of a common set of new challenges among the nanoelectronic devices provides an initial contribution to address the fundamental questions regarding the construction of nanoelectronic systems. Essentially, the highly shrunk dimensions and the severe unreliability in nano devices introduce significant changes in the design optimization considerations of the current CMOS based systems.

Specifically, in nanoelectronic system design, on the one hand, the hardware constraint becomes less stringent due to the abundance of resources introduced by the shrinking of transistor sizes; on the other hand, reliability needs to be addressed as a fundamental issue, thus presenting an important new dimension into the design optimization space. The most fundamental challenge that has emerged in constructing a workable nanoelectronic system is to enable reliable computations despite the severe unreliability imposed by the underlying nanoelectronic devices. On top of the reliability challenge, a number of particular characteristics that are significantly distinct for nanoelectronics, such as the strict interconnect constraint, the regularity in structure as a result of the bottom-up fabrication, the reconfigurability required to form essentially any operational functionality of the system, interacting with the fault tolerance aspect, will influence the design and CAD tools for the future nanoelectronic systems.

3 Dissertation Work

My dissertation focuses on the fundamental reliability challenge in constructing nanoelectronic systems. On the one hand, a number of new design issues need to be addressed when the fabric contains a massive number of defective components. On the other hand, the system needs to incorporate aggressive fault tolerance mechanisms at run time, including 1) the online monitoring of fault occurrence, followed by a timely self repairing process, or alternatively, 2) fault masking schemes.

The construction of any electronic system essentially relies on the organization of components at various hierarchy levels of the design. Therefore, under the nanoelectronic environment, fault tolerance mechanisms at various design hierarchy levels need to be taken into consideration. Although all the fault tolerance schemes need to exploit redundancy, either in the forms of hardware, time or information, the applicability of these techniques differs significantly across the design hierarchy levels of a system. Therefore, exploitation of various forms of redundancy engenders the possibility of intelligent tradeoffs between hardware and performance overheads.

I have carried out research work on various design hierarchy levels:

- Logic level:

The strict topological constraints in the length and connectivity of nanowires as well as the defective fabrication process lead to a fundamental difference between a nanoelectronic regular logic from the currently utilized regular structure based logic, which can assume fully connected and defect-free fabric. Due to such constraints, the mapping of a function onto a nanoelectronic fabric, namely logic mapping, during the logic synthesis process emerges as a new challenge in defect prone nano crossbar structures, since the logic function will fail once mapped to a defective part of the fabric. Consequently, it is essential to match the logic function to the underlying nanofabric according to some specific topological constraints. To address this problem, I have constructed the mathematical

model in a bipartite graph representation and developed a corresponding algorithm, which forms an important initial step for logic synthesis in the nanoelectronic environment [16].

To address the reliability problem in nanoelectronic logic systems, I have developed two schemes, based on two main types of fault tolerance approaches, namely online reconfiguration and fault masking, for a crossbar structure based nanoelectronic PLA logic. By specifically focusing on the dominant fault of missing nanoelectronic devices at the cross-points and exploiting the particularity of the logic implemented in the PLA structure, the two schemes not only exhibit complementary advantages, but also achieve significant fault tolerance capabilities with highly reduced hardware overhead [17].

For future research in this direction, I plan to work on large scale logic mapping with fault tolerance designs. Due to the NP-complete complexity of the logic mapping problem, searching for a solution in large scale logics becomes extremely expensive. Solving such a challenge for complex logic functions therefore requires CAD approaches to partition both the logic function and the nanofabric with insightful knowledge of their underlying structure.

Within the context of the nanoelectronic environment, the interconnectivity within the crossbar structure imposes significant influence on the search complexity and duration of such logic mapping processes. However, by adding a certain amount of redundancy in the logic implementation, it is possible to utilize extra area to compensate for the lack of interconnectivity of the underlying crossbar. This approach direction is quite promising since hardware resources in nanoelectronic systems are relatively abundant, especially in the regular structure based nano fabrics.

Furthermore, hardware redundancy is required for the fault tolerance logic design. Therefore, a further challenge involves the utilization of redundant hardware for both fault tolerance purposes and logic mapping for complex functions. I am interested in developing efficient CAD methodologies for general logic function mapping on the defective nanoelectronic regular structures with the consideration of fault tolerance.

- Arithmetic component level:

At the arithmetic component level, my research mainly focuses on adders, which constitutes the most basic arithmetic component building block. The fault tolerance approaches are essentially developed through: 1) exploiting the existing redundancy in the arithmetic components so as to achieve effective fault tolerance capabilities; 2) extending the application of time redundancy based approaches from the traditional fault detection area to the online fault diagnosis function so as to support reconfiguration based fault tolerance; 3) exploiting the new characteristics in nanoelectronic devices such as RTD and molecular electronic devices for the benefit of effective fault tolerance approaches.

1. Online repair based fault tolerance

Carry Lookahead Adders (CLA) exhibit high potential for the nanoelectronic environment due to their high performance and regular structure. I have developed a precise component-level fault identification scheme, which facilitates further online reconfiguration based fault tolerance schemes.

The reconfigurability supported by various nanoelectronic devices makes online repair a promising fault tolerance approach with high flexibility. A reconfiguration based online repair approach is composed of three stages: fault detection, fault diagnosis and reconfiguration based repair process. In my dissertation work, I have proposed a number of fault identification schemes for online diagnosis of faulty components with high precision. These techniques provide a basis for applying online repair fault tolerance approaches, for arithmetic blocks with regular components [18].

My future work in this direction involves developing online repair strategies based on the information in the diagnosis phase. Specifically, the main challenges in carrying out an efficient online repair process consist of the following aspects: (1) the design of reliable, hardware efficient control mechanism in carrying out the reconfiguration process; (2) topology aware organization of spare components as well as reconfiguration.

2. Information redundancy based fault tolerance

A number of emerging nanoelectronic devices, such as RTD and molecular electronic technologies, display the promising feature of supporting the implementation of multi-valued logics, thus facilitating the application of Carry Save Adders (CSA), which is not widely utilized in today's binary dominated CMOS systems. The fast computation in CSA is achieved by absorbing carry propagation within the redundant representation of the underlying number system. The obviation of carry propagation not only has the advantage of constant delay in the arithmetic datapaths, but also provides the potential of applying information redundancy to achieve fault tolerance. Based on the particularity of the CSA computation process, I have developed an information redundancy based fault tolerance scheme for the CSA components, thus enabling a unified coding based fault tolerance scheme across multiple subsystems including memory, buses and arithmetic components [19].

- Processor architecture level:

At the processor level, fault tolerance focuses on the circumstances where execution of instructions is extremely susceptible to runtime faults. Flexibility in fault tolerance is particularly crucial at this level due to two main reasons. On the one hand, flexibility needs to be introduced in dealing with the clustering and time varying behavior of faults. On the other hand, the topological constraint of the nanoelectronic environment needs to be considered in the traditional N Modular Redundancy (NMR) based approaches, where flexibility in terms of redundancy sharing among neighboring components is necessitated.

Computational models for nanoelectronic processor architectures should satisfy two core requirements. First, correctness of computations is a fundamental requirement. The overall system should operate reliably even though the computational units might produce incorrect results due to the occurrence of online faults. A second requirement is high performance: the large number of computational units should be used to dramatically speed up system performance. Based on the two core requirements, I have developed a processor architectural level computational model which addresses the unique challenges in a nanoelectronic environment: (i) How to translate the speedup afforded by nanoelectronic devices into high performance at the processor level and (ii) How to organize the abundant computational resources to trade off fault tolerance against system performance in the presence of high and time varying failure rates [20, 21, 22].

Traditional N-modular redundancy (NMR) exploits the large device densities offered by nanoelectronics for fault tolerance purposes. However, such approaches need to be specifically reconsidered for the nanoelectronic environment, where two main characteristics dominate: first, the fault rate is tremendously high with possible clustering and variable behaviors; second, nanofabrics are constrained to form in a regular structure due to fabrication limitation reasons, enforced reconfigurability and localized interconnections. Therefore, not only does flexibility need to be introduced for the traditional NMR approaches but furthermore needs to be constructed suitably for the regular structures. In my dissertation work, I have developed an adaptive NMR approach regarding the topological constraint of the nanoelectronic environment, consisting of: (i) a genre of nanofabric topologies that supports sharing of redundancies in the NMR approach so as to adapt to the time varying fault rates and (ii) reconfiguration algorithms for these topologies to deal with fault tolerance loss caused by manufacturing defects and operation-time online faults, respectively [23].

Based on the fault tolerance computational model I have developed in the thesis work, I am interested in the research of the following directions:

1. Developing online control mechanisms to monitor the behavior of faulty computational components. Based on the combined approach of time and hardware redundancy, online analysis can be performed to distinguish transient faults and permanent faults in the computational components. This information can be further utilized to trigger the self-diagnosis and repair control at the lower level of arithmetic components.
2. Integrate the topology consideration into the fault tolerant computational unit allocation.

In summary, the main research approaches I have developed regarding the construction of a reliable nanoelectronic system are based on the following principles:

- Developing fault tolerance schemes based on the consideration of the new characteristics exhibited by the emerging nanoelectronics. Particularly:
 1. A set of characteristics, such as the high and variable fault rates, regular structure and localized interconnections, impose severe constraints on the fault tolerance approaches.
 2. Other characteristics, such as reconfigurability and support for multi-valued logic, provide the potential to develop particular fault tolerance schemes that are efficient in hardware or performance.
- Cost-effective fault tolerance schemes rely on the exploitation of the existing redundancies in the system, rather than creating additional redundancies. Such a goal can be achieved through careful investigation of the specific component structures as well as unified coding based techniques across multiple subsystems.

4 Future Work

The design of nanoelectronic system opens a highly exciting new research area with various disciplines such as nanotechnology, electronic engineering, material science, biology, computer science and engineering closely involved. The highly challenging task of successfully constructing the future nanoelectronic systems demands not only intensive investigation in each of the discipline, but also broad understanding, significant amount of interaction and cooperation among the multiple disciplines.

I am eager to carry out my future research work in pushing the development of this new area with extensive communication and cooperation with the research experts across multiple disciplines and universities. My vision of the interdisciplinary communication to expedite the development of nanoelectronic systems focuses on the following directions:

- The construction of a nanoelectronic system needs to be based on the characteristics of the devices. Therefore, it is important for the system architects to learn from the nanotechnology, material science and electronic engineering disciplines the emerging developments in devices, so as to identify the specific challenges and resources for a nanoelectronic system.
- The constraints and optimization strategies at the multiple design hierarchy levels for the nanoelectronic systems can provide valuable information for device and transistor specifications. Particularly, an overall analysis of reliability versus hardware and performance overhead for a nanoelectronic system provides crucial evaluation metrics for the multiple candidates at the device level.
- CMOS devices, with well developed design and manufacturing techniques, are envisioned to be integrated with the nanoelectronic devices in future nanoelectronic systems. Consequently, the design of the nanoelectronic systems requires communication and cooperation among the research groups from multiple disciplines as nanotechnology, electronic engineering and electronic design automation.

I am highly interested in carrying out a number of long term research directions through cooperation among related research fields across multiple disciplines.

- **Fault behavior examination and related fault tolerance approaches**

The eventual delivery of a reliable nanoelectronic system depends heavily on the development of fault tolerance approaches, the effectiveness of which relies essentially on the in-depth understanding of fault behaviors in the nanoelectronic environment. Specifically, a number of fault behaviors such as the correlation and clustering behavior, transient / permanent characteristics, thermal impact on fault rates and testing damage for the devices are crucial to the development of fault tolerance techniques at various design hierarchy levels. I am anticipating to work with the research groups in the nanoelectronic device level in developing fault models according to the device characteristic specifications, so as to enable the development and precise parameterization of fault tolerance schemes for the nanoelectronic systems.

- **Reliability evaluation across multiple hierarchical levels** The overall reliability of a nanoelectronic system is associated with both the device characteristics and the multiple fault tolerance approaches at various design hierarchy levels. An evaluation of the overall fault tolerance capability is challenging, due to the involvement of multiple design hierarchy levels, with different fault tolerance techniques applicable on alternative designs and various components. However, an extensive reliability assessment from the system level can provide valuable insights for the design tradeoff spaces of the system, which can be used as feedback to direct the assessments of the device candidates. Consequently, I plan to develop an evaluation system which takes into consideration multiple design optimization dimensions in the nanoelectronic environment, namely reliability, performance and hardware resources, and actively interact with the research groups in various nanoelectronic device candidates. In the long run such a process will significantly expedite the realization of nanoelectronic systems.
- **Logic design with combined nanoelectronic / CMOS devices:** Nanoelectronic devices and the current CMOS devices have shown significant differences in terms of advantages and challenges in multiple aspects, such as reliability, density, fabrication, etc. Whether the future electronic system can be successful in delivering high performance reliably at low cost to a great extent relies on the design of a hybrid system consisting of both nanoelectronic and CMOS devices.

My long term research goal is to develop design methodologies and CAD tools which take into consideration both CMOS and nanoelectronics. Within this goal, the challenges mainly exist in the interface design for CMOS/nanoelectronic devices, as well as the decomposition of a component into the CMOS/nanoelectronic devices, as these aspects have crucial importance in the optimality of system performance, cost and reliability. To overcome such challenges, specific knowledge regarding the characteristics and fabrication of nanoelectronic devices across the disciplines of CAD, electronic engineering and nanoelectronic devices are required.

- **Novel computational model investigation for nanoelectronic systems:** The drastically different characteristics exhibited in a number of nanoelectronic device candidates have shown the potential of supporting non-traditional computational models for building electronic systems, such as neural network, cellular non-linear network, probabilistic logic gate, quantum computing, etc. I am interested in investigating novel computational models by collaborating with related areas of computer science and physics in my long term research program. In the near future, such novel computational models are applicable to particular modules and applications, such as image processing and prime number factorization. In the long run, the research and investigation of new computational models certainly will contribute to the forming of the future nanoelectronic systems, by eventually fully exploiting the potential provided by the molecular level devices.

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